

FIG. 1

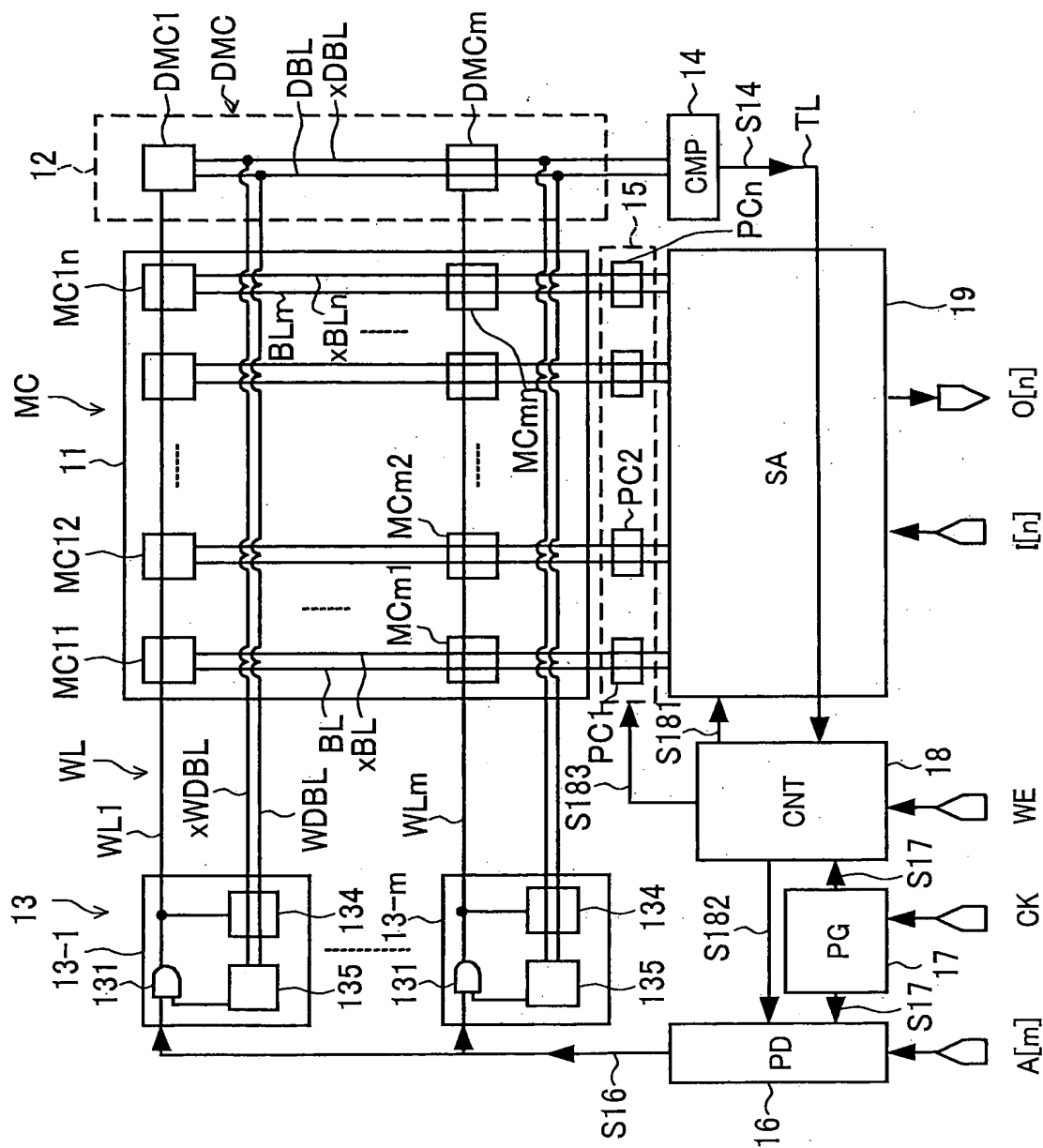
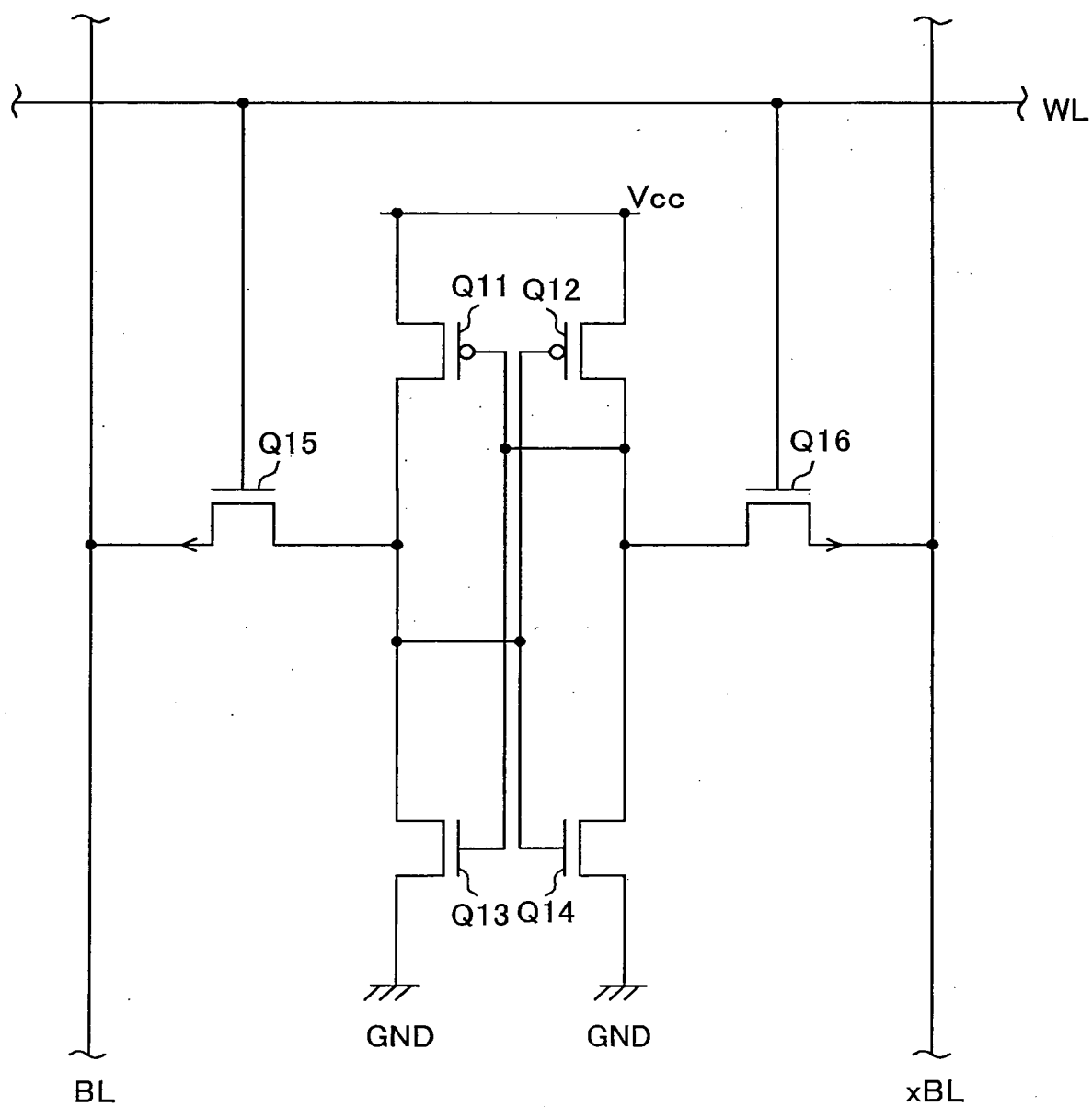
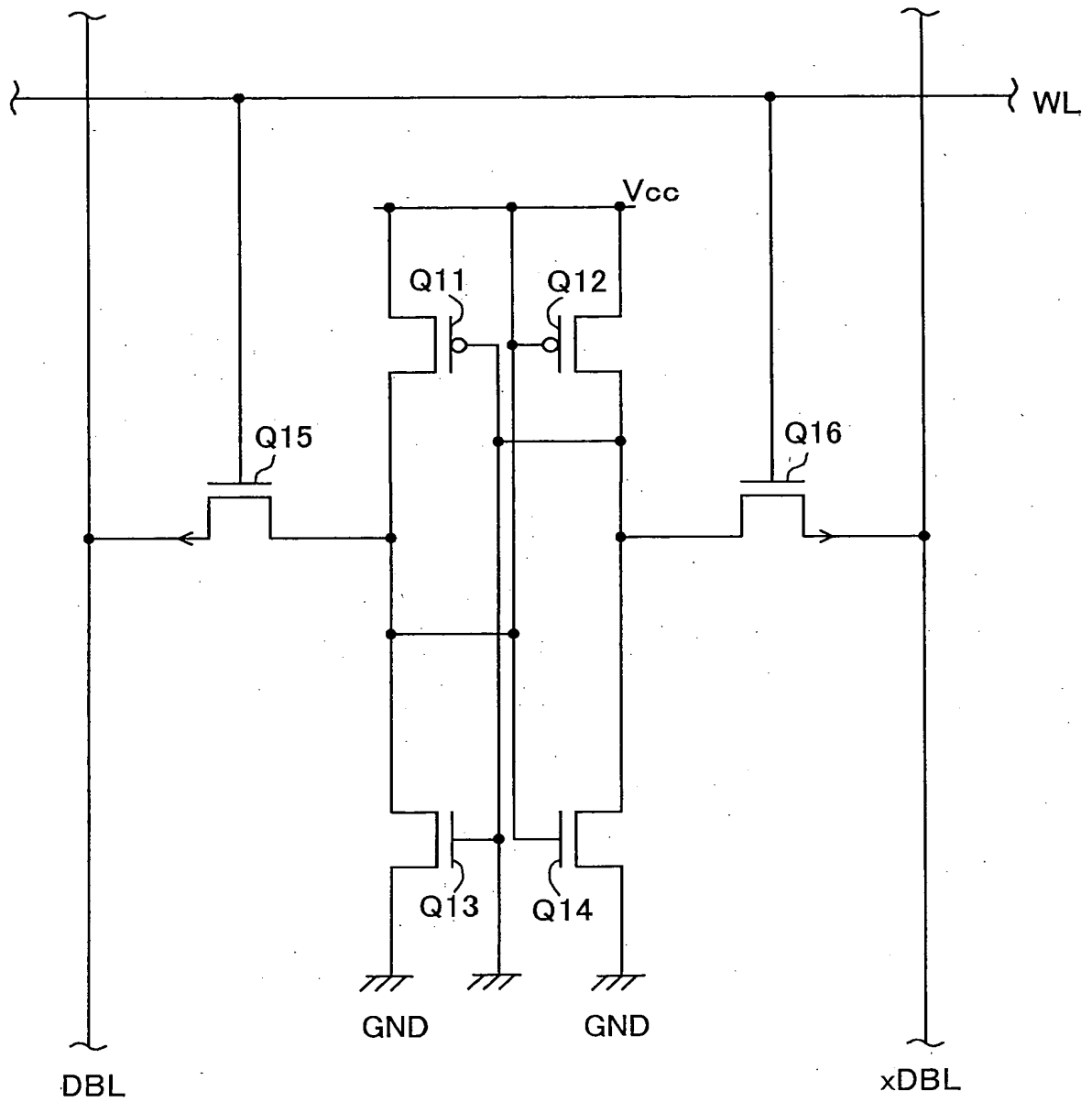


FIG. 2



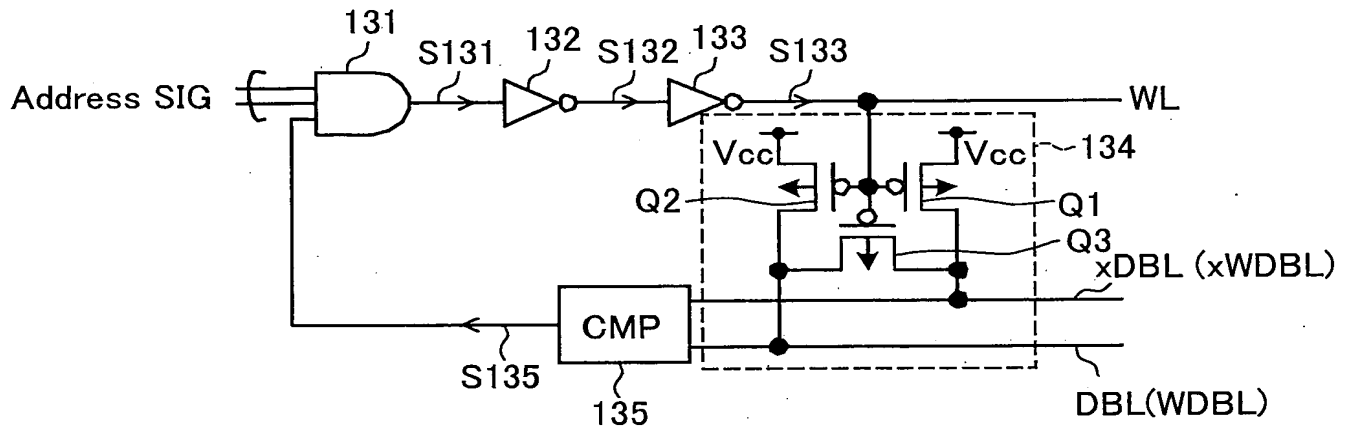
MC

FIG. 3



DMC

FIG. 4



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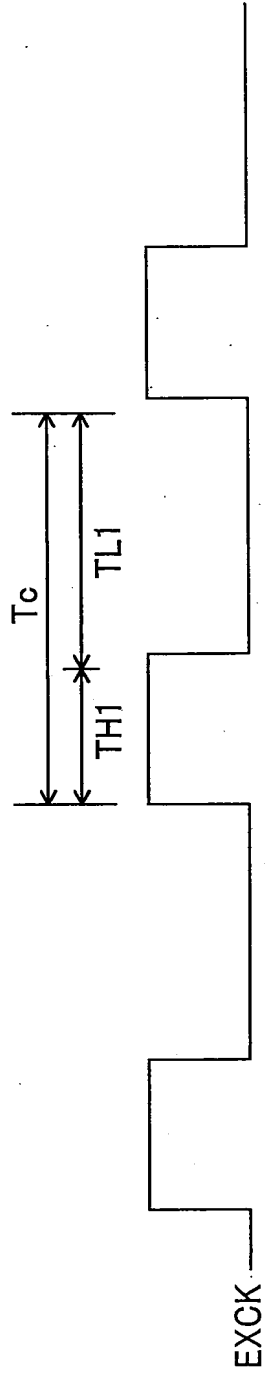


FIG. 5A

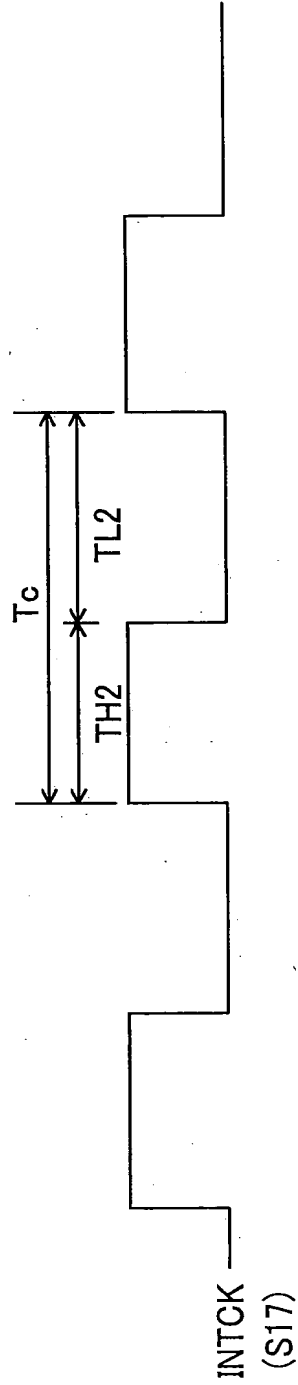
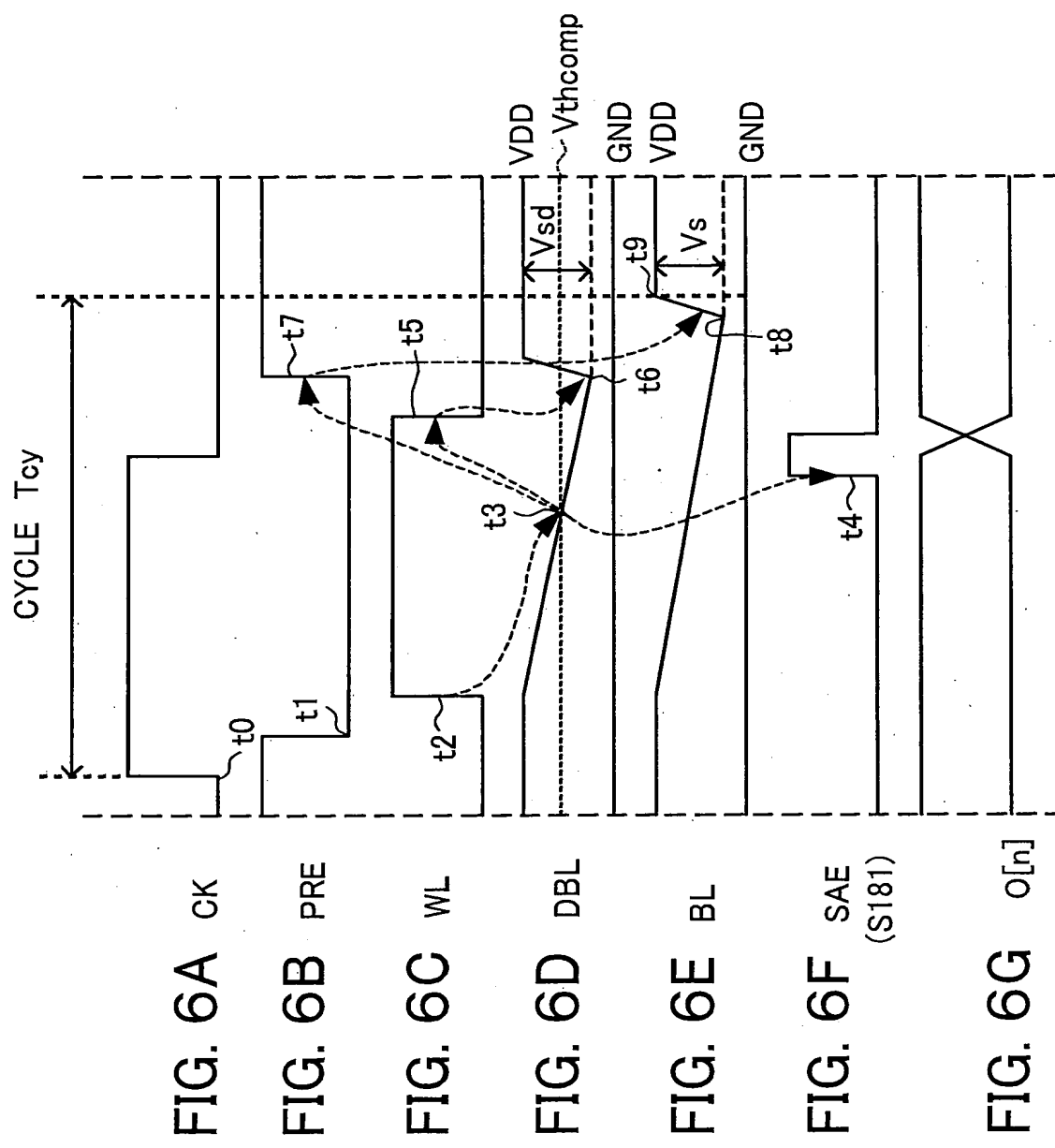


FIG. 5B



**FIG. 7**

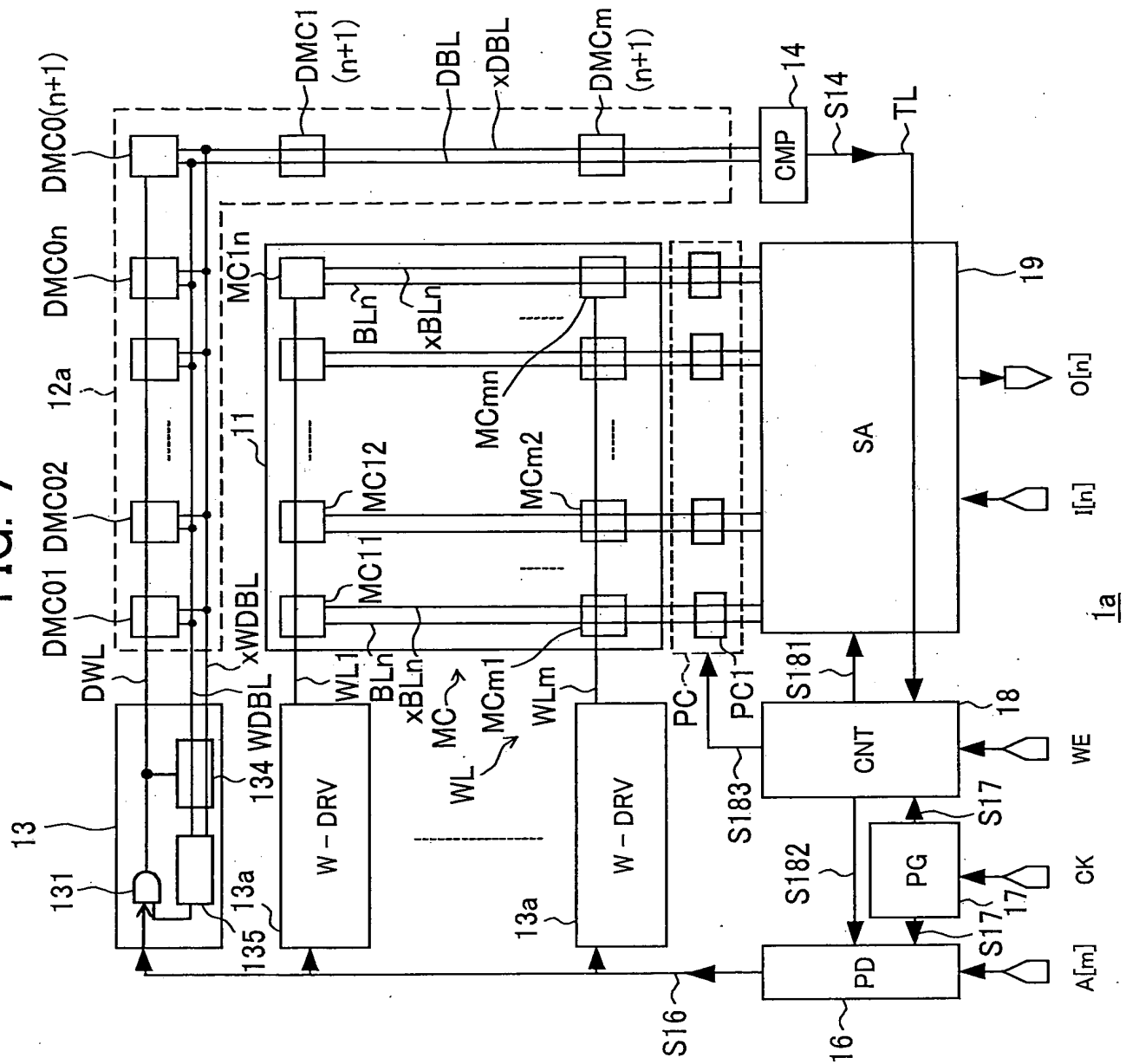
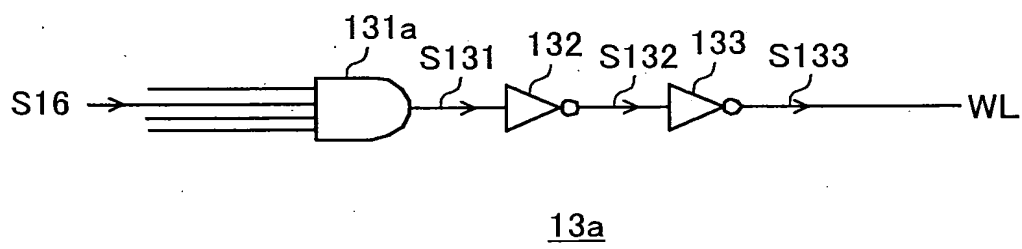
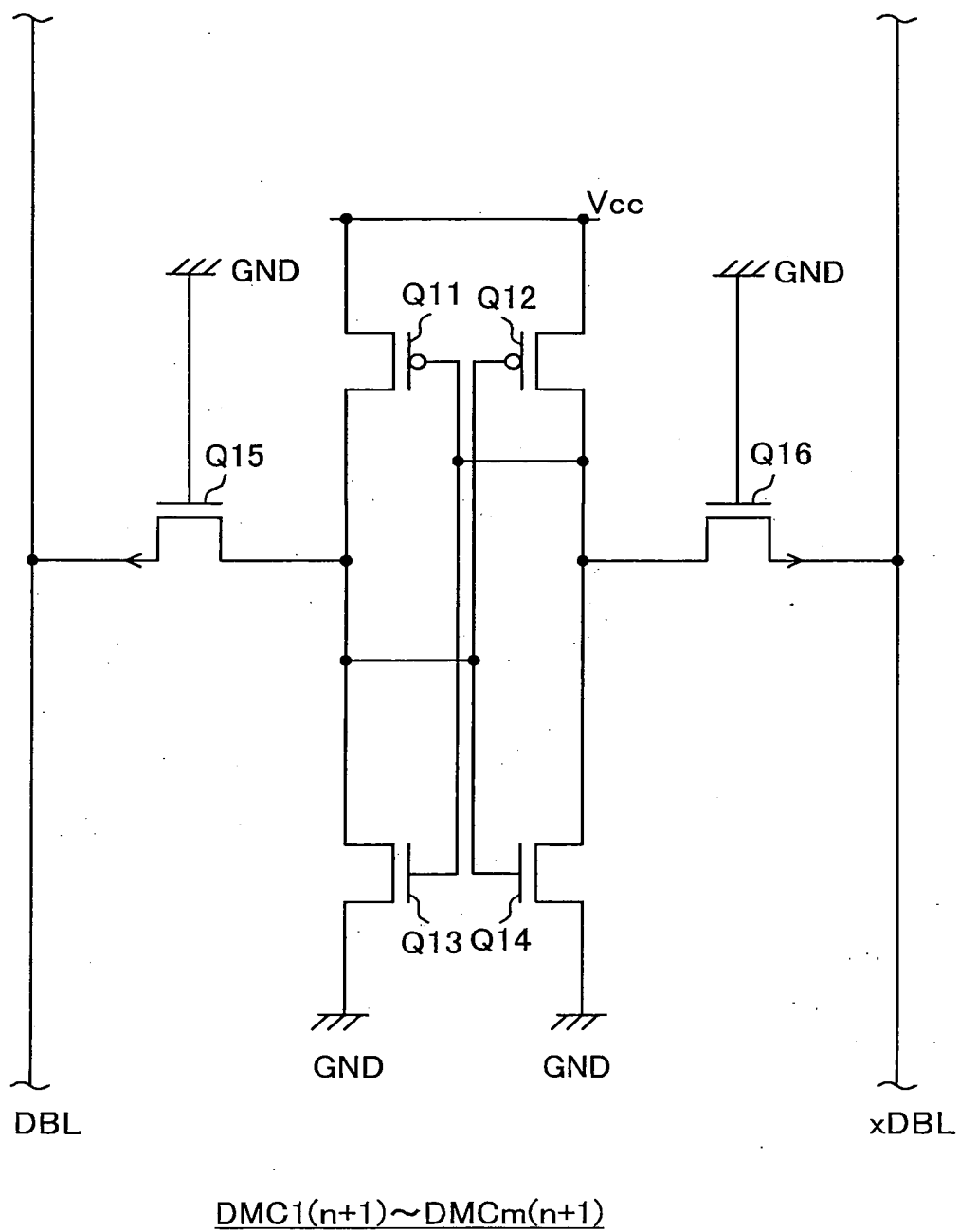


FIG. 8





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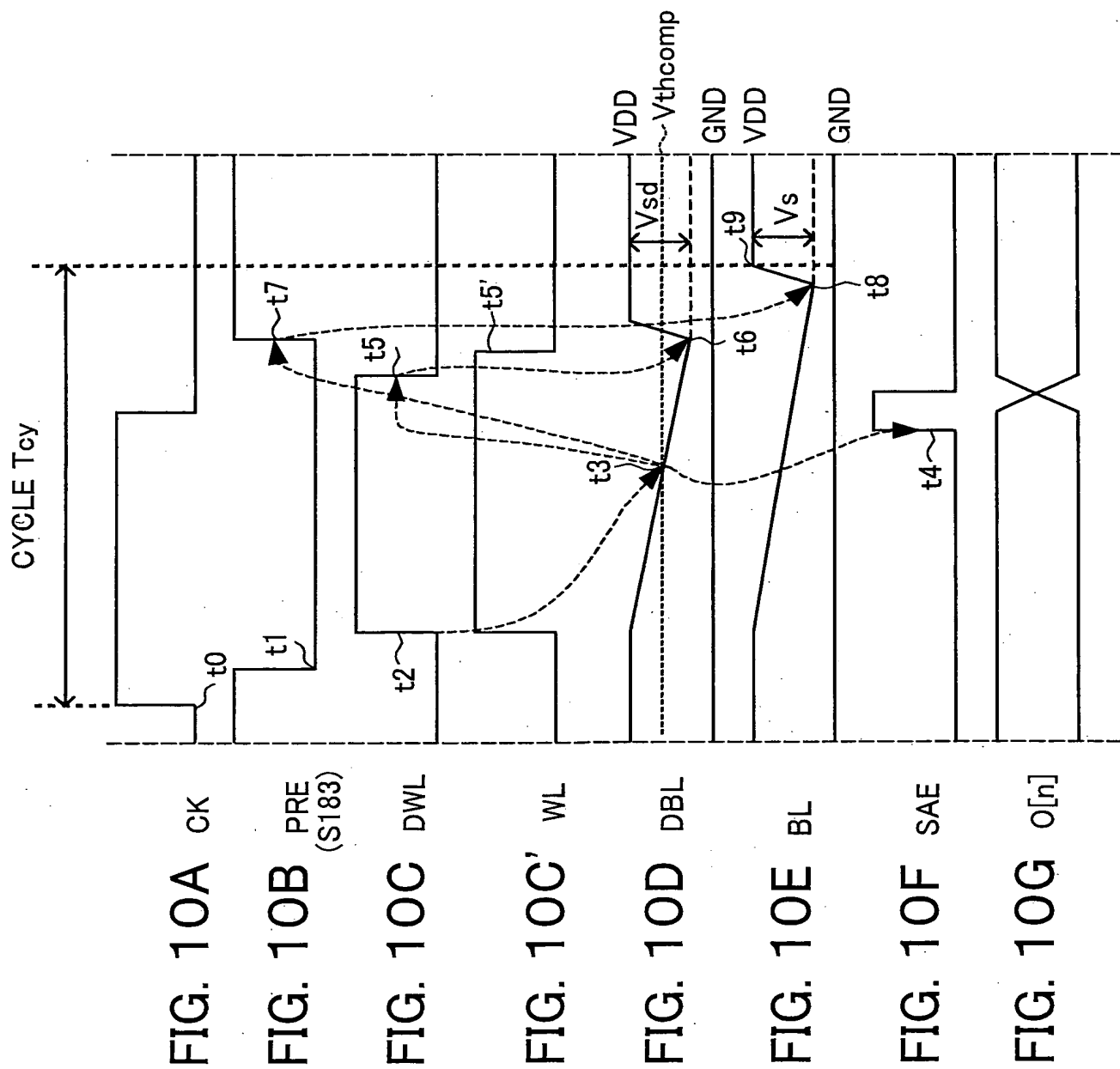
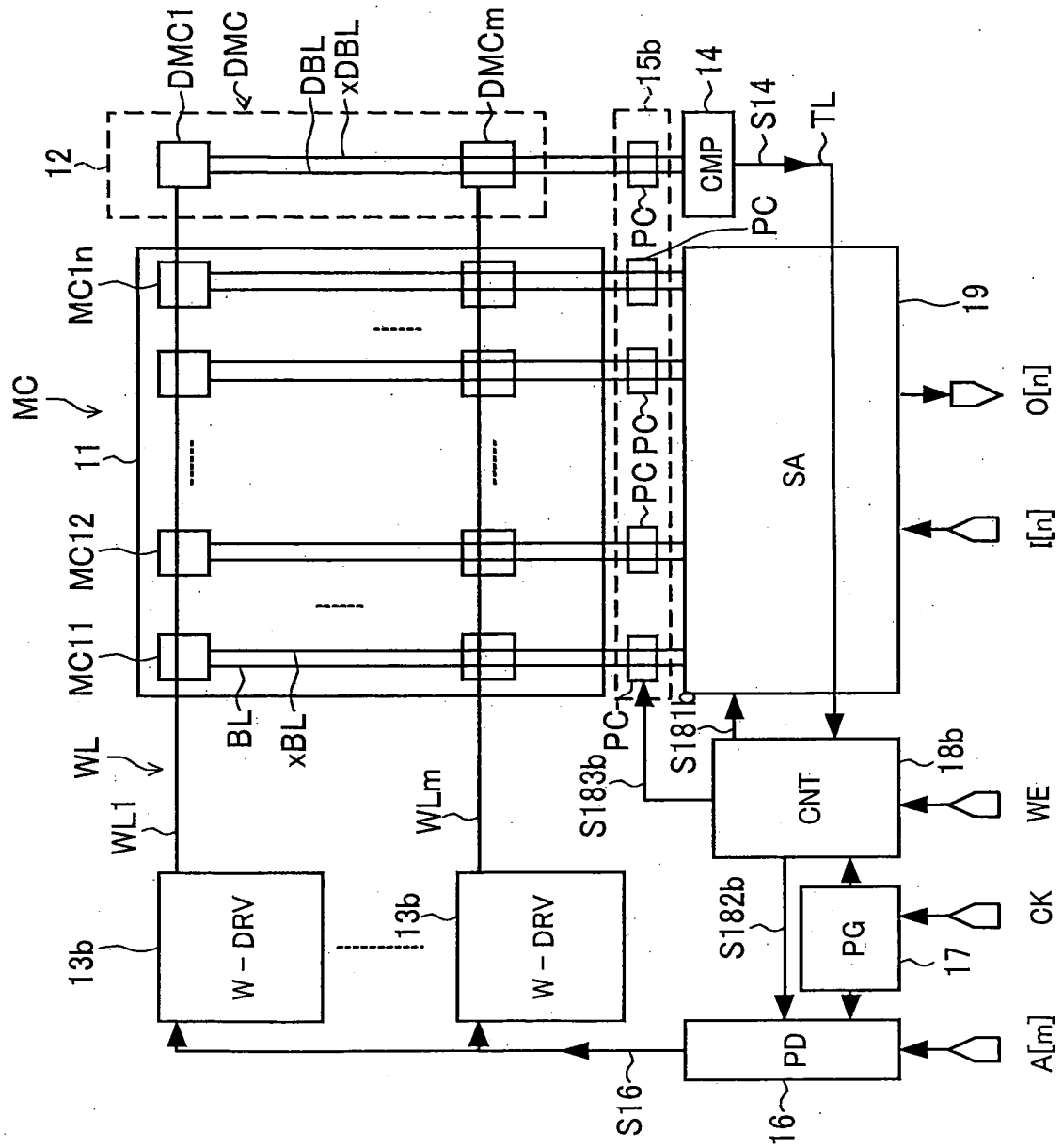
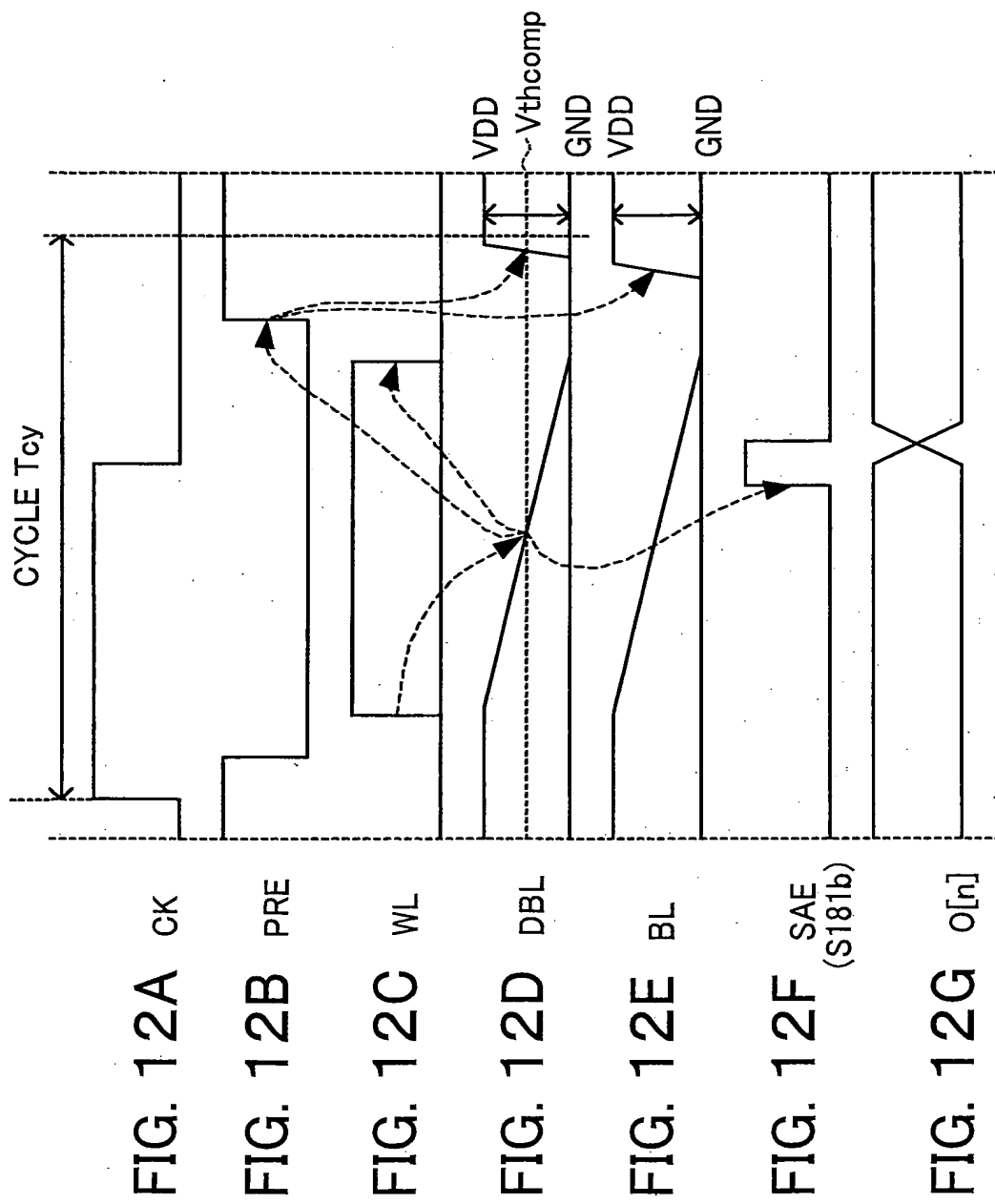


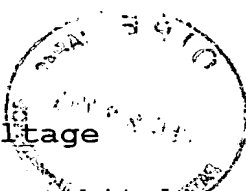
FIG. 11





## DESCRIPTION OF NOTATIONS

1, 1a... semiconductor memory device  
11... memory cell  
12... dummy memory cell  
13, 13a... word line driver  
14... comparator unit  
15... precharge circuit  
16... predecoder  
17... pulse generating unit  
18... internal timing control circuit  
19... sense amplifier  
131... AND gate  
132, 133... inverter  
134... precharge circuit  
135... comparator unit  
A[m]... input address signal  
BL<sub>n</sub>, xBL<sub>n</sub>... bit line  
CK... clock signal  
DBL, xDBL... dummy bit line  
DMC... dummy memory cell  
DWL... dummy word line  
MC... memory cell  
PC... precharge circuit  
Q1 to Q3, Q11 to 16... transistor  
TL... timing line



Vcc... power source voltage

WDBL, xWDBL... word dummy bit line

DWL... dummy word line

WL... word line